



Dual-Rate Speech Coder for the TMS320C6000

Commetrex' 60094-2 speech coder is a resource-efficient implementation of the ITU G.723.1 on the Texas Instruments TMS320C6000 family of DSPs. G.723.1 is widely deployed in H.324 conferencing systems and PSTN-IP gateways where high-quality speech and low-bandwidth utilization are requirements.

G.723.1 specifies coding schemes that compress 64-KBPS PCM speech to either 5.3- or 6.3-KBPS. The lower-bit-rate coder uses "algebraic-code-excitation linear prediction" (ACELP) as the coding scheme; the higher-bit-rate coder uses "multi-pulse maximum-likelihood excitation" (MP-MLQ). Each coder is designed to process frames of 240 samples, or 30-milliseconds of speech data. It is possible to switch between the two rates on any 30-msec frame boundary.

The 60094-2 speech coder includes the silence compression specified in G.723.1 Annex A. Voice-activity detection (VAD) and comfort-noise generation are included.

60094-2 is eXpress DSP Compliant (http://dspvillage.ti.com/docs/express_dsp/expressdsphome.jhtml). The TMS320DSP Algorithm Standard is directly supported by the MSP Consortium M.100 specification (<http://www.msp.org>) so it is compatible with any MSP-conforming media-processing system.

Features

- Low resource utilization
- C-callable interface
- Does not disable interrupts
- TMS320DSP Algorithm Standard compliant
- MSP Consortium M.100 compatible

Benefits

- High densities
- Low power
- Low implementation cost

'C6000 Resource Utilization

6.3K Encoder: 10.0 MCPS
 6.3K Decoder: 1.4 MCPS (with post filter)
 5.3K Encoder: 11.9 MCPS
 5.3K Decoder: 1.33 MCPS (with post filter)
 Program Memory (full duplex): 82,400 bytes
 Tables: 11,736 bytes
 Per-Instance Memory: 2160 bytes

License Options

Limited-Use Paid-Up Source Code
 Royalty with Reduced Up-Front
 Object Code with Runtime Licenses

Ordering Information

60094-2 G.723.1 for the TI TMS320C6000

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